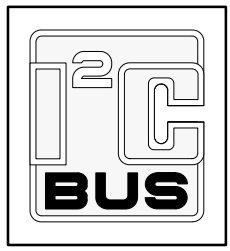
DATA SHEET



P82B715
I²C bus extender

Product data
Supersedes data of 2003 Feb 20

2003 Dec 02

Philips
Semiconductors

PHILIPS

I²C bus extender P82B715

DESCRIPTION

The P82B715 is a bipolar IC intended for application in I²C bus systems. While retaining all the operating modes and features of the I²C system it permits extension of the practical separation distance between components on the I²C bus by buffering both the data (SDA) and the clock (SCL) lines.

The I²C bus capacitance limit of 400 pF restricts practical communication distances to a few meters. Using one P82B715 at each end of a long cable (connecting Lx/Ly to Lx/Ly) reduces the cable loading capacitance on the I²C bus by a factor of 10 times and allows the total system capacitance load (all devices, connectors, traces and wires that are connected to the I²C bus) to be around 3000 pF. That means longer cables or lower cost general purpose wiring may be used to connect two separate I²C based systems without worrying about the special voltage levels associated with other I²C bus buffers. Multiple P82B715s can be connected together in a star or multi-point architecture by their Lx/Ly ports without limit as long as the total capacitance of the system remains less than about 3000 pF (400 pF or less when referenced to any Sx/Sy connection). In that arrangement the master and/or slave devices are attached to the Sx/Sy port of each P82B715. The P82B715 alone does not support voltage level translation but it simplifies the application of low cost transistors for this purpose. There is no restriction on interconnecting the Sx/Sy I/Os and those I/Os are also fully compatible with bus buffers that use voltage level offsets (i.e., PCA9511, PCA9515, Sx/Sy side of P82B96) because it duplicates and transmits the offset voltage.

FEATURES

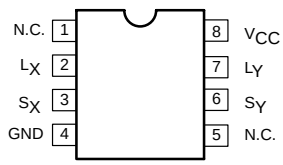
- Dual, bi-directional, unity voltage gain buffer with no external directional control required.
- I²C Bus compatible
- Logic signal levels may include (but not exceed) both supply and ground
- Logic signal input voltage levels are output without change and are independent of V_{CC}
- X10 impedance transformation, but does not change logic voltage levels.
- Supply voltage range 3 V to 12 V
- Clock speeds to at least 100 kHz and 400 kHz when other system delays permit
- ESD protection exceeds 2500 V HBM per Mil. Std 883C-3015.7 and 400 V MM per JESD22-A115. (I/Os have diodes to V_{CC} and GND)
- Latch-up free (bipolar process with no latching structures)

TYPICAL APPLICATIONS

- Increase the total connected capacitance of an I²C system to around 3000 pF (see AN255 appendix 2)
- Drive I²C signals over long cables to approximately 50 meters or 3000 pF
- When used in pairs allows, for example, 200 pF on each Sx/Sy I/O plus 2000 pF on the linked Lx/Ly I/Os
- Drives x10 lower impedance bus wiring for improved noise immunity
- Multi-drop distribution of I²C signals using low cost twisted-pair cables

PIN CONFIGURATIONS

8-Pin Dual In-Line or SO
P82B715



SU00290

PINNING

PIN	SYMBOL	FUNCTION
1	N.C.	No connection
2	L_X	Buffered Bus, LDA or LCL
3	S_X	I²C Bus, SDA or SCL
4	GND	Negative Supply
5	N.C.	No connection
6	S_Y	I²C Bus, SCL or SDA
7	L_Y	Buffered Bus, LCL or LDA
8	V_{CC}	Positive Supply

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
8-pin plastic dual In-line package	-40 to +85 °C	P82B715PN	P82B715PN	SOT97-1
8-pin plastic small outline package	-40 to +85 °C	P82B715TD	P82B715	SOT96-1

NOTES:
1. For applications requiring lower voltage operation, or additional buffer performance, see AN255 I²C and SMBus Repeaters, Hubs and Expanders Application Note.
2. Standard packing quantities and other packaging data are available at www.philipslogic.com/packaging.

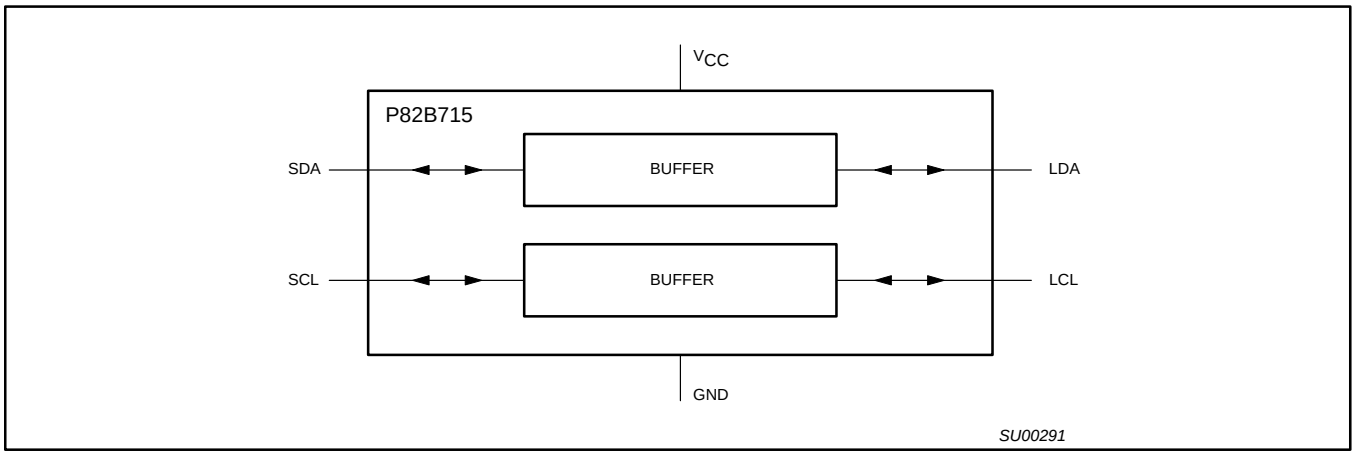


Figure 1. Block Diagram: P82B715

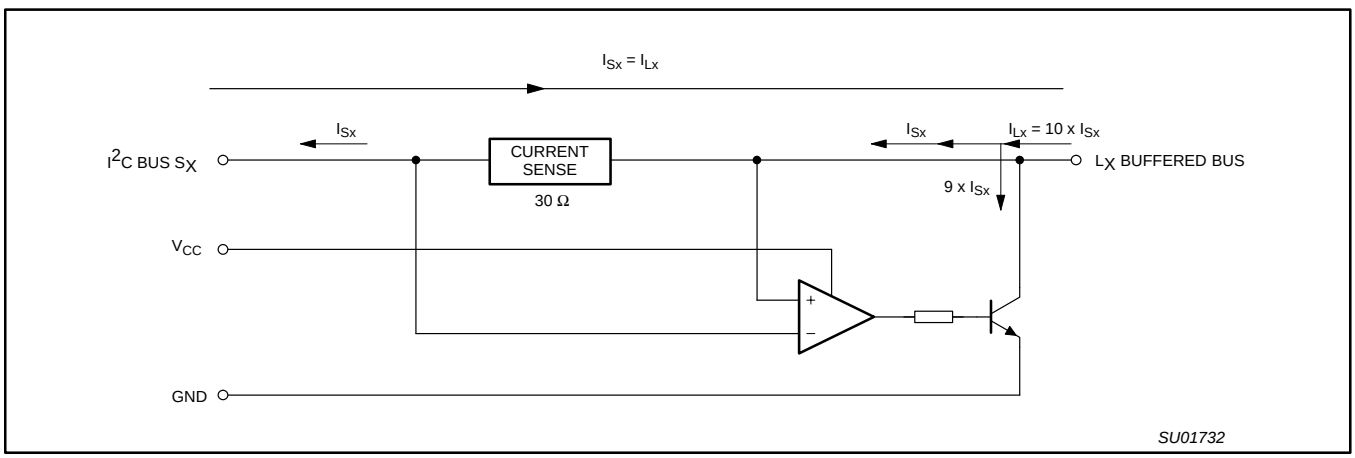


Figure 2. Equivalent Circuit: One Half P82B715

Sx, Sy, I²C-Bus, SDA or SCL

On the normal side, because the two buffer circuits in the P82B715 are identical, either the Sx or Sy input pins can be used as the I²C Bus SDA data line, or the SCL clock line.

Lx, Ly, Buffered Bus, LDA or LCL

On the special low impedance or buffered line side, the corresponding output becomes the LDA data line or LCL clock line.

V_{CC}, GND — Positive and Negative Supply Pins

In normal use the power supply voltages at each end of the low impedance buffered bus line should be the same. If these differ by a significant amount, noise margin is sacrificed.

FUNCTIONAL DESCRIPTION

The P82B715 bipolar integrated circuit is a dual bi-directional logic signal driver that increases the allowable total I²C system wiring capacitance. It contains identical circuits, one for each bus signal, and requires no external directional control. It uses unidirectional analog current amplification to increase the current sink capability of I²C chips by a factor 10 and to change the 400 pF I²C bus specification limit into a 4nF bus wiring capacitance limit. This allows I²C, or similar bus systems, to be extended over long distances without degradation of system performance or the use of special cables.

P82B715 provides current amplification from its I²C bus to its low impedance or buffered bus. Whenever current is flowing out of Sx, into an I²C chip driving the I²C bus low, its amplifier will sink ten times that current into Lx to drive the buffered bus low (see Figure 2).

To minimize interference and ensure stability, the current rise and fall times of the Lx drive amplifier are internally controlled.

The P82B715 does not amplify signal currents flowing into Sx on the I²C bus, driven by currents flowing out of Lx on the buffered side. A buffered bus logic low signal at Lx passes via the internal 30 Ω resistor to drive the I²C bus low.

This signal current amplification, dependent on its direction, preserves the multi-master, bi-directional, open-collector/open-drain, characteristic of any connected I²C bus lines and the new low impedance bus. Bus logic signal voltage levels will be clamped at (Vcc + 0.7 V) but otherwise are independent of the supply voltage Vcc.

APPLICATION NOTES

By using two (or more) P82B715 ICs, a sub-system can be built that retains the interface characteristics of a normal I²C device so that the sub-system may be included in, or added onto, any I²C or related system.

The sub-system features a low impedance or buffered bus, capable of driving large wiring capacitance (see Figure 3).

The P82B715 will operate with a supply voltage from 3 V to 12.5 V but the logic signal levels at Sx/Lx are independent of the chip's supply. They remain at the levels presented to the chip by the attached ICs. The maximum static I²C bus sink current, 3 mA, flowing in either direction in the internal current sense resistor, causes a difference less than 100 mV in the bus logic low levels at Sx and Lx. This makes P82B715 fully compatible with all logic signal drivers, including TTL. The P82B715 cannot modify the bus logic signal voltage levels but it contains internal diodes connected between Lx/Sx and Vcc that will conduct and limit the logic signal swing if the applied logic levels would have exceeded the supply voltage by more than 0.7 V.

In normal applications external pull-up resistors will pull the connected buses up to the desired voltage high level. Usually this will be the chip supply, Vcc, but for very low logic voltages it is necessary to use a Vcc of at least 3.3 V and preferably higher. Note that full performance over temperature is only guaranteed from 4.5 V. Specification de-ratings apply when its supply voltage is reduced below 4.5 V. The absolute minimum Vcc is 3 V.

I²C Systems

As in standard I²C systems, pull-up resistors are required to provide the logic high levels on the buffered bus. (The standard open-collector configuration is retained). The size and number of pull-up resistors depends on the system.

If P82B715 ICs are to be permanently connected into a system, the circuit may be configured with only one pull-up resistor on the buffered bus and none on the I²C buses, but the system design will be simplified and performance improved by fitting separate pull-ups on each section of the bus. When a sub-system using P82B715 may be optionally connected to an existing I²C system that already has a pull-up then the effects of the sub-system pull-ups acting in parallel with the existing I²C bus pull-up must be considered.

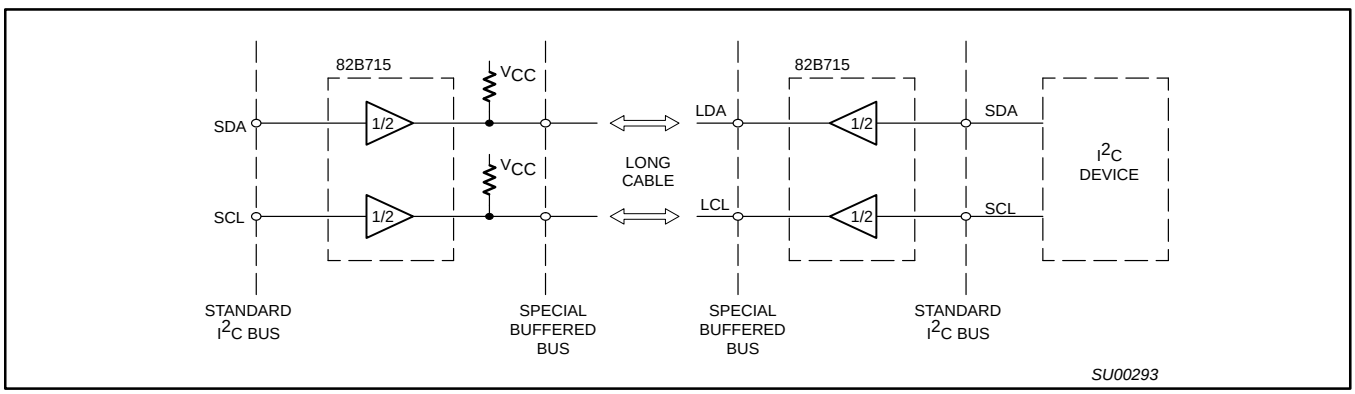


Figure 3. Minimum Sub-System with P82B715

Pull-Up Resistance Calculation

When calculating the pull-up resistance values the gain of the buffer introduces scaling factors which must be applied to the system components. In practical systems the pull-up resistance value is calculated to meet the rise time limit for I²C systems. As an approximation, this limit will be satisfied in a 100 kHz system if the time constant of the total system (product of the net resistance and net capacitance) is set to 1 microsecond or less.

In systems using the P82B715 it is convenient to set the total system time constant by considering each bus node separately (i.e., the I²C nodes and the buffered bus node)and selecting a separate pull-up resistor for each node to provide time constants of less than 1 microsecond. If each node complies then the system requirement is also met.

This arrangement, using multiple pull-ups as in Fig 4, provides the best system performance and allows stand-alone operation of individual I²C buses if parts of the extended system are disconnected or re-connected. For each bus section the pull-up resistor is calculated as follows:

$$R = \frac{1\mu s}{C\ device + C\ wiring}$$

Where: C device = sum of any connected device capacitances, and C wiring = total wiring and stray capacitance on the bus section.

[The 1 µs is an approximation, with a safety factor, to the theoretical time-constant necessary to meet the specified 1 µs bus rise-time specification in a system with variable logic thresholds where the CMOS limits of 30% and 70% of Vcc apply. The calculated value is 1.18 µs.]

If these capacitances cannot be measured or calculated then an approximation can be made by assuming that each device presents 10 pF of load capacitance and 10 pF of trace capacitance and that cables range from 50 to 100 pF per metre.

If only a single pull-up must be used then it must be placed on the buffered bus (as R2 in Fig 4) and the associated total system capacitance calculated by combining the individual bus capacitances into an equivalent capacitive loading on the buffered bus.

This equivalent capacitance is the sum of the capacitance on the buffered bus plus 10 times the sum of the capacitances on all the connected I²C nodes. The calculated value should not exceed 4 nF. The single buffered bus pull-up resistor is then calculated to achieve the 1 µs risetime and it then provides the pull-up for the buffered bus and for all other connected I²C bus nodes included in the calculation.

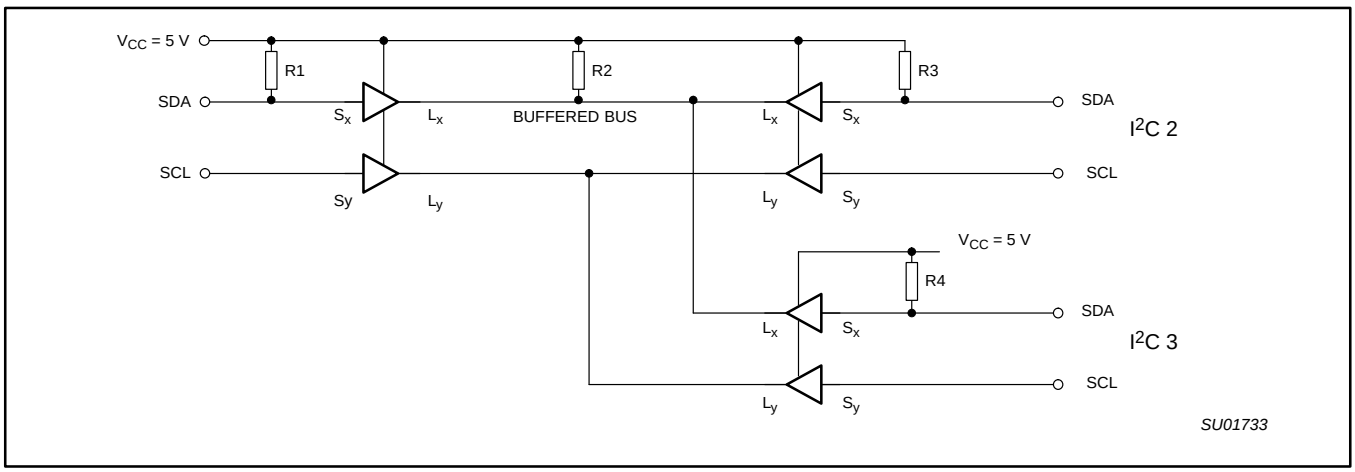


Figure 4. Single Pull-up Buffered Bus

Calculating bus drive currents

Figure 4 shows three P82B715s connected to a common buffered bus. The associated bus capacitances are omitted for clarity but assume the resistors have been selected to give R-C products of less than 1 µs so the bus rise time requirement is satisfied. An I²C chip connected at I²C 1 and holding the SDA bus low must sink the current flowing in its local pull-up R1 plus, with assistance from the P82B715, the currents in R2, R3 and R4. Because the resistors R3 and R4 act to pull the bus nodes I²C 2 and I²C 3, and their corresponding Sx pins, to a voltage higher than the voltage at the Lx pins their buffer amplifiers will be inactive. The SDA at Sx of I²C 2 and I²C 3 is pulled low by the low at Lx via the internal 30 ohm resistor that links Lx to Sx. So the effective current that must be sunk by the P82B715 buffer on I²C 1, at its Lx pin, is the sum of the currents in R2, R3 and R4. The Sx current that must be sunk by an I²C chip at I²C 1, due to the buffer gain action, is 1/10 of the Lx current. So the effective pull-up, determining the current to be sunk by an I²C chip at I²C 1, is R1 in parallel with resistors 10 times the values of R2, R3 and R4. If R1 = R3 = R4 = 10k, and R2 = 1k, the effective pull-up load at I²C 1 is 10k||10k||100k||100k = 4.55 k ohms

The same calculation applies for I²C 2 or I²C 3.

To calculate the current sunk by the Lx pin of the buffer at I²C 1 note that the current in R1 is sunk directly by the IC at I²C 1. The buffer therefore sinks only the currents flowing in R2, R3, and R4 so the effective pull-up is R2 in parallel with R3 and R4.

In this example that's 1k||10k||10k = 833 ohms. For a 5.5 V supply and 0.4 V low that means the buffer is sinking 16.3 mA.

The P82B715 has a static sink rating of 30 mA at Lx. The requirement is that the pull-up on the buffered bus, in parallel with all other pull-ups that it is indirectly pulling low on Sx pins of other P82B715 ICs, will not cause this 30 mA limit to be exceeded.

The minimum pull-up resistance in a 5 V +/-10% system is 170 ohms.

The general requirement is:

$$\frac{V_{CC}\ max - 0.4}{R_P} < 30\ mA$$

Where: Rp = parallel combination of all pull-up resistors driven by the Lx pin of the P82B715.

Figure 5 shows calculations for an expanded I²C bus with 3 nF of cable capacitance.

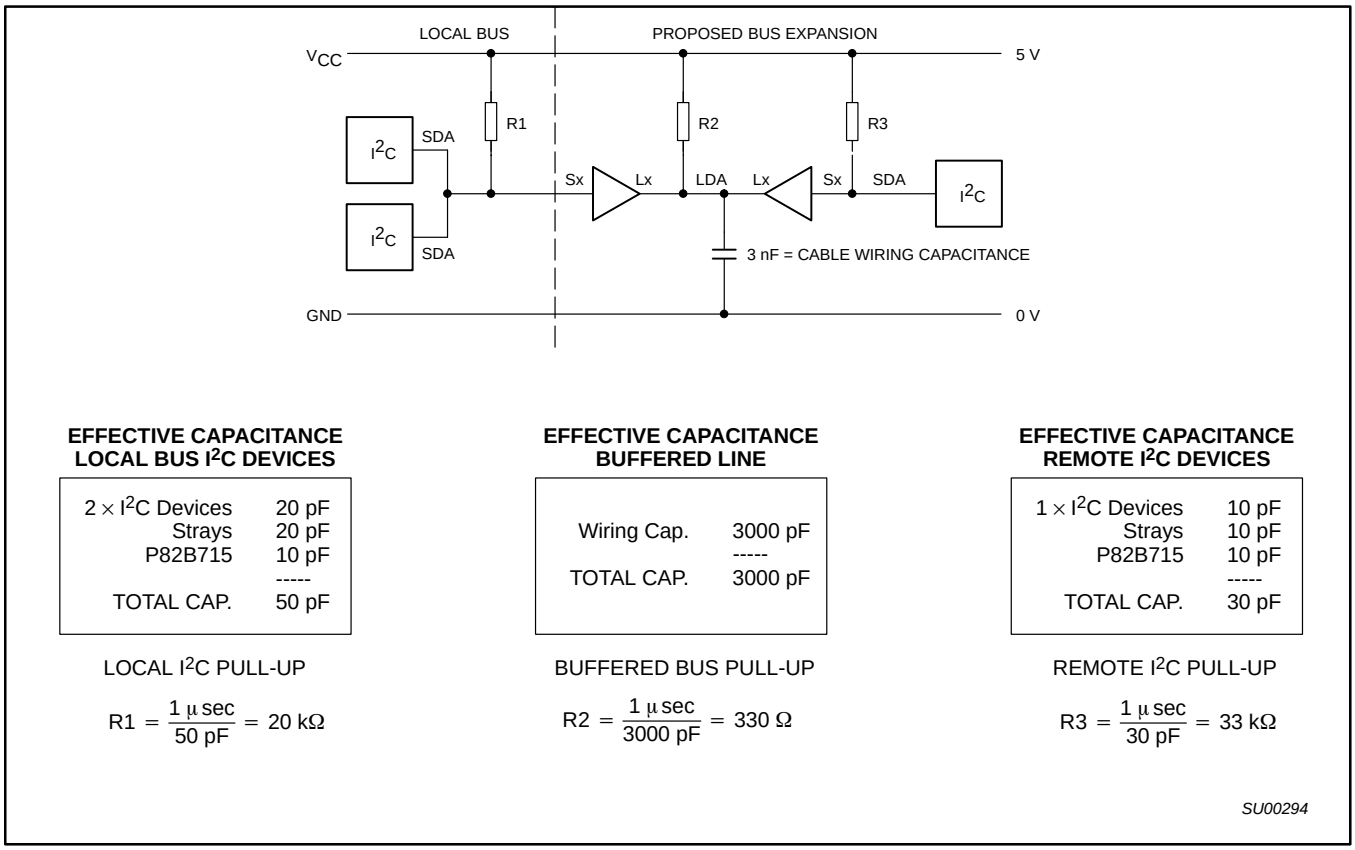


Figure 5. Typical Loading Calculation: Adding An Extension Bus with P82B715

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Voltages with respect to pin GND (DIL-8 pin 4).

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
V_{CC} to GND	Supply voltage range V_{CC}	-0.3	+12	V
V_{bus}	Voltage range I²C Bus, SCL or SDA	0	V_{CC}	V
V_{buff}	Voltage range Buffered Bus	0	V_{CC}	V
I	DC current (any pin)	—	60	mA
P_{tot}	Power dissipation	—	300	mW
T_{stg}	Storage temperature range	-55	+125	°C
T_{amb}	Operating ambient temperature range	-40	+85	°C

CHARACTERISTICS

At T_{amb} = +25 °C and V_{CC} = 5 Volts, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.	MAX.	
Power Supply					
V_{CC}	Supply voltage (operating) (Note 1)	4.5	—	12	V
I_{CC}	Supply current	—	14	—	mA
I_{CC}	Supply current at V_{CC} = 12 V	—	15	—	mA
I_{CC}	Supply current, both I²C inputs LOW, both buffered outputs sinking 30 mA.	—	22	—	mA
Drive Currents					
I_{Sx}, I_{Sy}	Output sink on I²C bus, V_{CC} > 3 V V_{Sx}, V_{Sy} LOW = 0.4 V V_{Lx}, V_{Ly} LOW on Buffered bus = 0.3 V and I_{LX}, I_{LY} = -3 mA (Note 2)	3	—	—	mA
I_{Lx}, I_{Ly}	Output sink on Buffered bus V_{Lx}, V_{Ly} LOW = 0.4 V V_{Sx}, V_{Sy} LOW on I²C-bus = 0.3 V	30	—	—	mA
De-rated Dynamic Drive Currents for V_{CC} < 4.5 V (Note 1)					
I_{Lx}, I_{Ly}	Output sink on Buffered bus, V_{CC} > 3 V V_{Lx}, V_{Ly} LOW = 0.4 V to 1.5 V I_{Sx}, I_{Sy} sinking on I²C-bus < -4 mA	24	—	—	mA
I_{Lx}, I_{Ly}	Output sink on Buffered bus, V_{CC} > 3 V V_{Lx}, V_{Ly} LOW = 1.5 V to V_{CC} I_{Sx}, I_{Sy} sinking on I²C-bus = -7 mA	24	—	—	mA
Input Currents					
I_{Sx}, I_{Sy}	Input current from I²C bus when I_{Lx}, I_{Ly} sink on Buffered bus = 30 mA	—	—	-3	mA
I_{Lx}, I_{Ly}	Input current from Buffered bus (V_{CC} > 3 V) when I_{Sx}, I_{Sy} sink on I²C bus = 3 mA (Note 2)	—	—	-3	mA
I_{Lx}, I_{Ly}	Leakage current on Buffered bus, V_{CC} = 3 V to 12 V V_{Lx}, V_{Ly} = V_{CC}, and V_{Sx}, V_{Sy} = V_{CC}	—	—	200	µA
Impedance Transformation					
Z_{in}/Z_{out}	Input/Output impedance V_{SX} < V_{LX} and buffer is active	8	10	13	
Buffer Delay Times					
$t_{rise/fall\ delay}$ I_{Sx} to V_{Lx} I_{Sy} to V_{Ly}	Time delay to V_{Lx} voltage crossing $V_{CC}/2$ for input drive current step I_{SX} at S_X, see Figure 6 (Note 3). R_{Lx} pull up = 270 Ω, no capacitive load, V_{CC} = 5 V	—	250	—	ns
$t_{rise/fall\ delay}$ V_{Lx} to V_{Sx} V_{Ly} to V_{Sy}	Buffer time delay of switching edges, between V_{Lx} input and V_{Sx} output (Note 4). R_{Sx} pull up = 4700 Ω, no capacitive load, V_{CC} = 5 V	—	0	—	ns

NOTES:

1. Operation with reduced performance is possible down to 3 V. Typical static sinking performance is not degraded at 3 V, but the dynamic sink currents while the output is being driven through $V_{CC}/2$ are reduced and can increase fall times. Timing-critical designs should accommodate the guaranteed minimums.
2. Buffer is passive in this test. The S_X/S_Y sink current flows via an internal resistor to the driver connected at the L_X/L_Y I/O.
3. A conventional input-output delay will not be observed in the S_X/L_X voltage waveforms because the input and output pins are internally tied with a 30 Ω resistor so they show equal logic voltage levels, to within 100 mV. When connected in an I²C system an S_X/S_Y input pin cannot rise/fall until the buffered bus load at the output pin has been driven by the internal amplifier. This test measures the bus propagation delay caused to falling or rising voltages at the L_X/L_Y output (as well as the S_X/S_Y input) by the amplifier's response time. The figure given is measured with a drive current as shown in Figure 6. Because this is a dynamic bus test, in which a corresponding bus driving IC has an output voltage well above 0.4 V, 6 mA is used instead of the static 3 mA.
4. The signal; path L_X to S_X and L_Y to S_Y is passive, via the internal 30 Ω resistor. There is no amplifier involved and essentially no signal propagation delay.

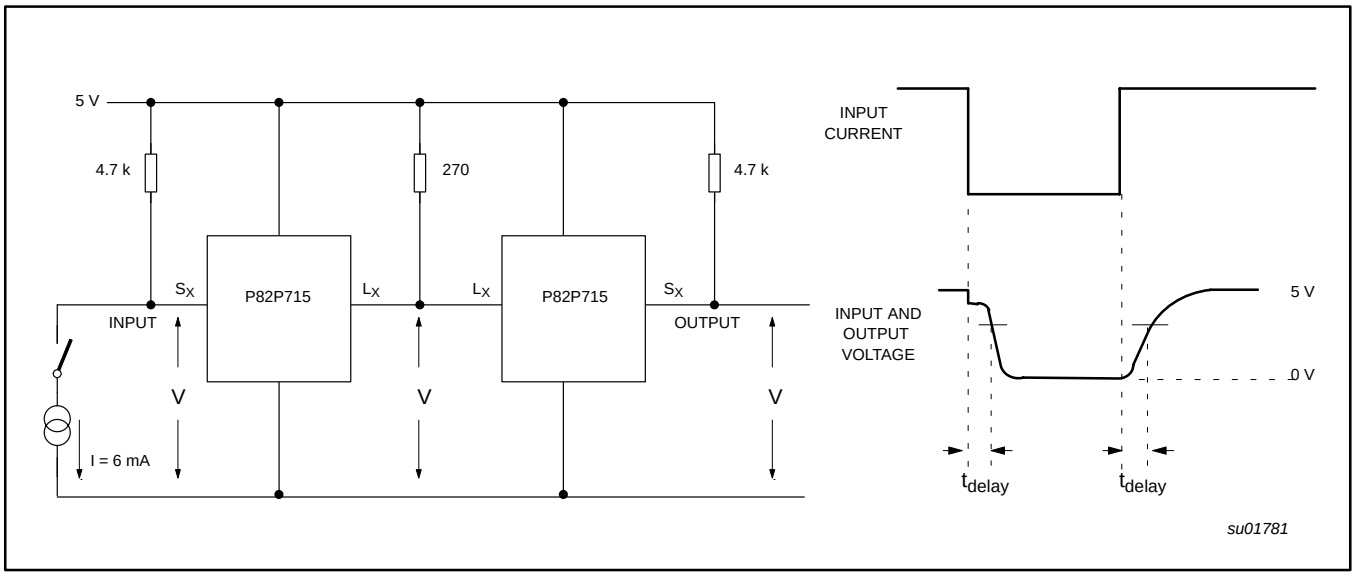
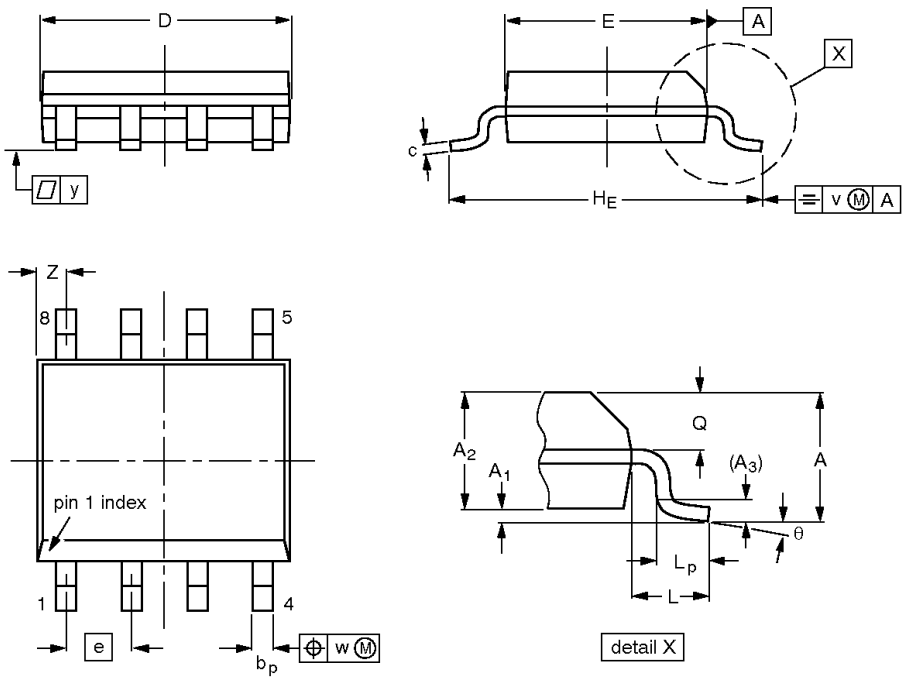
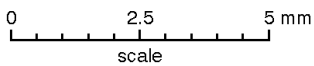


Figure 6. Test circuit for delay times

SO8: plastic small outline package; 8 leads; body width 3.9 mm SOT96-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

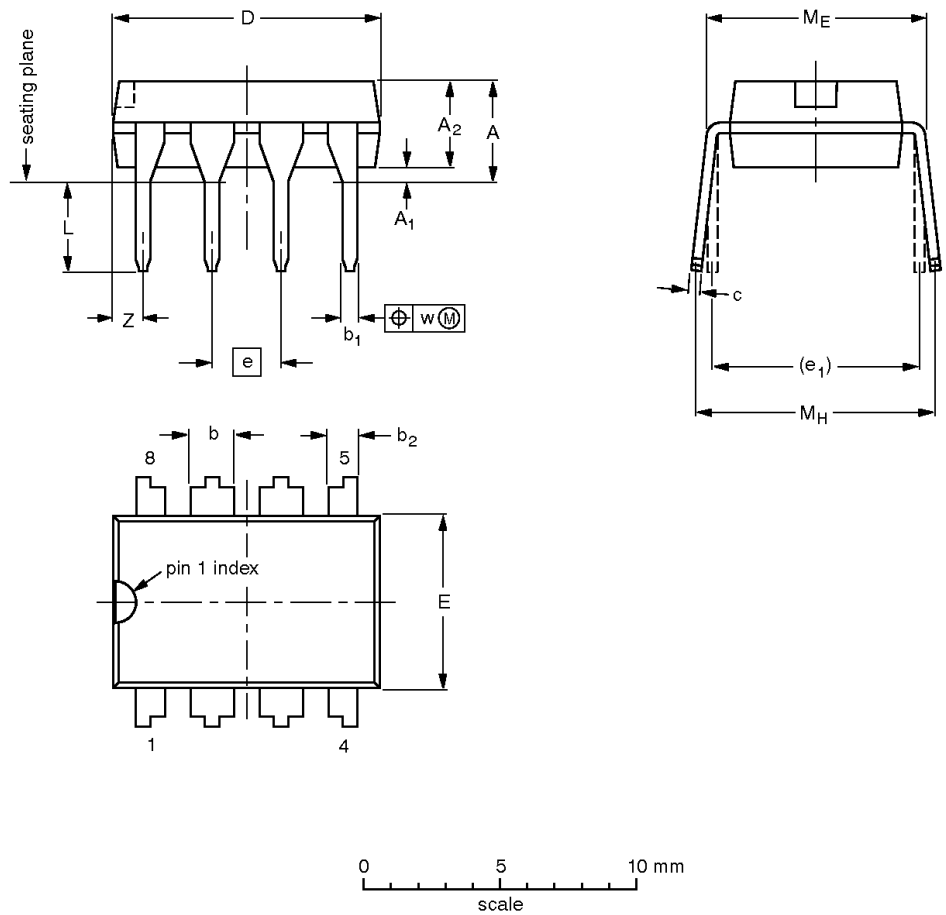
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.02	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT97-1	050G01	MO-001	SC-504-8			~~99-12-27~~ 03-02-13

REVISION HISTORY

Rev	Date	Description
_6	20031202	**Product data (9397 750 12452); ECN 853-2240 01-A14516 of 14 November 2003; supersedes data of 2003 Feb 20 (9397 750 11094).** Modifications: • Description and application information was added and limits on the devices preformance were pulled in.
_5	20030220	**Product data (9397 750 11094); ECN 853-2240 29410 of 22 January 2003; supersedes data of 2001 Mar 06 (9397 750 08163).**
_4	20010306	**Product data (9397 750 08163); ECN 853-2240 25757 of 2001 Mar 06.**

I²C bus extender P82B715

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Level	Data sheet status[1]	Product status[2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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